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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Atty. Dkt. No: 5310-04500

Inventor(s):
Daniel Bois
Thomas Skotnicki
Malgorzata Jurczak

Title: SEMICONDUCTOR DEVICE COMBINING THE ADVANTAGES OF MASSIVE AND SOI ARCHITECTURE, AND METHOD FOR MAKING SAME

CERTIFICATE OF EXPRESS MAIL
UNDER 37 C.F.R. §1.10

"Express Mail" mailing label number EL 764353659 US
DATE OF DEPOSIT March 29, 2002

I hereby certify that this paper (along with any paper and/or fee referred to as being attached or enclosed) is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to
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Washington, D.C. 20231

Shayna Blackmar

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

INTERNATIONAL APPLICATION NO.: PCT/FR00/02710
INTERNATIONAL FILING DATE: September 29, 2000
PRIORITY DATE CLAIMED: October 1, 1999
U.S. APPLICATION NO. (If known): Unknown

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. § 371.

2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. § 371.

3. ☐ This is an express request to begin national examination procedures (35 U.S.C. § 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. § 371(b) and PCT Articles 22 and 39(l).

4. ☒ A translation of the International Application into English (35 U.S.C. § 371(c)(2)), including a title page, 10 pages of specification, 2 pages of claims (claims 1-10), and a 1 page abstract.

5. ☒ Drawings
☒ Formal Figure(s) 1-5 on 6 sheet(s).

6. ☒ A copy of the International Application as filed (35 U.S.C. § 371(c)(2))
☐ is transmitted herewith including: 1 page abstract..
☒ has been transmitted by the International Bureau.
☒ A copy of Form PCT/IB/308 (1 page) is enclosed.
☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

7. ☒ A copy of the International Publication, Publication No. WO 01/26160.

8. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. § 371(c)(3))
   - ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   - ☐ have been transmitted by the International Bureau.
   - ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - ☐ have not been made and will not be made.
   - ☐ a translation of the amendments to the claims are transmitted here with.

9. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
   - ☐ A copy of the Demand for International Preliminary Examination is enclosed.

10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. § 371(c)(4)):
   - ☐ is enclosed (_____ pages).
   - ☐ a combined Declaration and Power of Attorney is enclosed (_____ pages).
   - ☒ is not enclosed. Applicant requests the Patent and Trademark Office to accept this application and accord a serial number and filing date as of the date this application is deposited with the U.S. Postal Service for Express Mail. Further, Applicant requests that the NOTICE OF MISSING PARTS-FILING DATE GRANTED be sent to the undersigned representative of Applicant.

11. ☒ Applicant hereby claims priority to:
   - ☒ International Application No.: PCT/FR00/02710 filed September 29, 2000.
   - ☒ French application No.: FR 99/12308 filed October 1, 1999.
   - ☒ A copy of Form PCT/IB/304 (1 page) indicating receipt of the priority document by the International Bureau is enclosed.

12. ☐ A translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. § 371(c)(5)).

13. ☒ The entire disclosure of the International Application referred to above is considered to be part of the accompanying application and is hereby incorporated by reference herein.

14. ☐ Assignment Papers.
   - ☐ An assignment document is enclosed for recording (_____ pages).
   - ☐ Form PTO-1595 Assignment Recordation Cover Sheet (page).

15. ☒ A Preliminary Amendment (6 pages).

16. ☒ A substitute specification for pages 1-10, 13(11 pages).

17. ☒ A strikethrough version of specification, claims, and abstract (14 pages).

18. ☐ Power of Attorney
   - ☐ Is enclosed.
   - ☐ a combined Declaration and Power of Attorney is enclosed.

19. ☒ Information Disclosure Statement (IDS), including:
   - ☒ Form PTO-1449
   - ☒ Reference(s) marked according to Form PTO-1449.

20. ☒ Return Receipt Postcard

21. ☐ Small Entity Status
   - ☐ A small entity statement is enclosed.

22. ☐ Copy of PCT Form PCT/IB/338

23. ☐ Copy of International Request.

24. ☒ Copy of International Preliminary Examination Report.
☒ A copy of the International Preliminary Examination Report in French.
☐ English Translation of the International Preliminary Examination Report.

25. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR § 1.492 (a) (1)-(5): ☐ Neither international preliminary examination fee nor international search fee paid to USPTO and International Search Report not prepared by the EPO or JPO.....$1040.00 ☒ International preliminary examination fee not paid to USPTO but International Search Report prepared by the EPO or JPO.....$890.00 ☐ International preliminary examination fee not paid to USPTO but international search fee paid to USPTO.....$740.00 ☐ International preliminary examination fee paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4).....$710.00 ☐ International preliminary examination fee paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4).....$100.00				
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Surcharge of $130.00 for furnishing oath or declaration later than ☐ 20 ☐ 30 Months from the earliest claimed priority date (37 C.F.R. § 1.492(e)).				
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	20 - 20 =	0	x $18.00 =	$0.00
Independent claims	3 - 3 =	0	x $78.00 =	
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TOTAL NATIONAL FEE:				$890.00
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☒ A fee authorization in the amount of $890.00 is enclosed.

☐ Please charge my Deposit Account No. 50-1505/ in the amount of to cover the above fees.

☒ The Commissioner is hereby authorized to charge any other fees which may be required or credit any overpayment to Conley, Rose, & Tayon, P.C., Deposit Account No. 50-1505/5310-04500/EBM.

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Signature

Name Eric B. Meyertons
Registration No. 34,876
Date

PATENT 5310-04500

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: Unknown §
Filed: Herewith §
Inventor(s): §
Daniel Bois §
Thomas Skotnicki §
Malgorzata Jurczak §
§
Title: SEMICONDUCTOR §
DEVICE COMBINING §
THE ADVANTAGES OF §
MASSIVE AND SOI §
ARCHITECTURE, AND §
METHOD FOR MAKING §
SAME §

Examiner: Unknown
Group/Art Unit: Unknown
Atty. Dkt. No: 5310-04500

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Commissioner for Patents
Box Patent Application
Washington, DC 20231

Shayna Blackmar

PRELIMINARY AMENDMENT

Commissioner for Patents
Box Patent Application
Washington, DC 20231

Sir:

Please amend the above-captioned application as follows:

In the Specification:

Please replace pages 1-10 of the specification with pages 1-10 of the enclosed substitute sheets. Applicant has also submitted herewith a strikethrough version of the specification indicating the amendments.

In the Claims:

Please amend the claims as follows. Applicant has also submitted herewith a strikethrough version of the claims indicating the amendments.

1. (Amended) A semiconductor device, comprising:

a silicon body, in which are formed source and drain regions defining between them a channel region;

a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer; and

a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer, wherein the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that the source and drain regions each overlap respectively, at least in part, one of said opposed zones.

2. (Amended) The device of claim 1, wherein the buried dielectric layer extends between the source and drain regions.

3. (Amended) The device of claim 1, wherein the buried dielectric layer extends over the entire surface of the silicon body below the source and drain regions.

4. (Amended) The device of claim 1, wherein the device has a planar structure.

5. (Amended) The device of claim 1, wherein the buried dielectric layer is an air-filled cavity.

6. (Amended) The device of claim 1, wherein the buried dielectric layer is a solid material.

7. (Amended) The device of claim 1, wherein the device is a transistor.

8. (Amended) A process for fabricating a device, comprising:

forming a germanium or SiGe alloy layer on a main surface of a silicon body;

forming a thin silicon layer on the germanium or SiGe alloy layer;

forming a thin gate dielectric layer on the thin silicon layer;

forming a gate on the gate dielectric layer and a hard mask on the gate;

forming first spacers on two opposed sides of the gate and of the hard mask, wherein the first spacers are made of a first material;

forming second spacers along the first spacers, wherein the second spacers are made of a second material different from the first material;

etching, on each side of the second spacers, of the gate dielectric layer, of the thin silicon layer, and optionally of part of the germanium or SiGe alloy layer;

selective etching of the germanium or SiGe alloy layer in order to form a tunnel;

optionally, filling the tunnel with a solid dielectric;

removing the second spacers in order to expose two zones on the thin silicon layer, wherein the two zones are located respectively on either side of the first spacers; and

forming source and drain regions on either side of the first spacers, wherein the source and drain regions overlap, at least in part, the two zones.

9. (Amended) The process of claim 8, wherein forming the source and drain regions comprises deposition of polycrystalline silicon by selective epitaxy in order to form polycrystalline silicon deposits on either side of the first spacers, wherein the polycrystalline silicon deposits are precursors of the source and drain regions and overlap, at least in part, the exposed zones of the thin silicon layer, and the method further comprising removing the gate hard mask and implanting a dopant in the polycrystalline silicon deposits in order to produce the source and drain regions.

10. (Amended) The process of claim 8, wherein forming the source and drain regions comprises deposition of a thick polycrystalline silicon encapsulating layer, forming a resin mask on the thick polycrystalline silicon layer, etching of the thick polycrystalline silicon layer to the desired shape and dimensions by means of the resin mask, removing of the resin mask, chemical-mechanical polishing of the thick silicon layer down to level with the gate in order to produce parts in the thick polycrystalline silicon layer which are intended to form the source and drain regions co-planar with the gate and implanting of a dopant in the parts in order to form the source and drain regions.

Please add the following claims:

11. (new) The device of claim 1, wherein the buried dielectric layer has a thickness between about 1 nm and about 50 nm.

12. (new) The device of claim 1, wherein the thin silicon layer has a thickness between about 1 nm and about 50 nm.

13. (new) The device of claim 1, wherein a length of the two opposed zones is less than about 100 nm.

14. (new) The device of claim 1, wherein the thin gate dielectric layer comprises SiO_2.

15. (new) The device of claim 1, wherein the source and drain regions lie in the same plane as the gate.

16. (new) The method of claim 8, wherein the SiGe alloy layer has a germanium fraction greater than about 0.1.

17. (new) The method of claim 8, wherein etching of the gate dielectric layer, of the thin silicon layer, or part of the germanium or SiGe alloy layer comprises plasma etching.

18. (new) The method of claim 8, wherein the first spacers comprise SiO_2 or Si_3N_4.

19. (new) The method of claim 8, wherein the second spacers comprise SiO_2 or Si_3N_4.

20. (new) A semiconductor device, comprising:

a silicon body, in which are formed source and drain regions defining between them a channel region;

a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer; and

a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer, wherein the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that the source and drain regions each overlap respectively, at least in part, one of said opposed zones, and wherein the buried dielectric layer extends between the source and drain regions.

In the Abstract:

Please replace the abstract with the enclosed substitute sheet. Applicant has also submitted herewith a strikethrough version of the abstract indicating the amendments.

It is believed that no fees are due in connection with the filing of this Preliminary Amendment. However, if any fees are due, the Commissioner is hereby authorized to deduct said fees from Conley, Rose & Tayon Deposit Account No. 50-1505/5310-04500/EBM.

Respectfully submitted,

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Date: 3/29/02

Substitute Version of Specification and Abstract

In the Specification:

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates in general to high-performance CMOS semiconductor devices for the rapid processing of signals and/or for low voltage/low-power applications, and more particularly to field-effect MOS transistors (MOSFETs). The novel architecture called "silicon-on-nothing" (SON) architecture combines the advantages of bulk and silicon-on-insulator (SOI) architectures.

2. Description of the Related Art

One of the limiting factors of conventional bulk-architecture MOSFETs is the substrate effect which impairs the properties of the transistor. This drawback is avoided in MOSFETs of silicon-on-insulator (SOI) architecture by separating the thin silicon film from the substrate by a buried silicon oxide layer.

Elimination of the substrate effect in MOSFETs of fully-depleted thin SOI film architecture may result in an increase in the drain current.

However, MOSFETs of ultra-thin SOI architecture suffer from a high source/drain (S/D) resistance because of shallow junctions limited by the thickness of the silicon layer and because of poor thermal conductivity. Furthermore, the cost of fabricating substrates of SOI architecture is high, which has limited their introduction on to the market.

SUMMARY OF THE INVENTION

To remedy the drawbacks of the devices of the prior art, a semiconductor device like that shown in Figure 1 has been proposed. This device inlcudes a silicon substrate 10, in which are formed source 23 and drain 24 regions, a thin gate dielectric layer 14 on

the channel region and a gate 15 on the thin gate dielectric layer 14, a buried layer 22 of a dielectric extending between the source and drain regions and a thin silicon layer 13 lying between the buried dielectric layer 22 and the gate dielectric layer 14, constituting the channel region of the device between the source and drain regions 23, 24. The buried dielectric layer 22 may consist of an air-filled cavity.

Because of the very small thickness of the thin silicon layer 13 constituting the channel, lateral contact of the source 23 and drain 24 regions with this silicon layer 13 is difficult to achieve.

An embodiment includes modifying the architecture of the junctions of the device described above, so as to make a reliable and easily producible contact between the thin silicon layer constituting the channel and the source and drain regions.

An embodiment also includes a process for producing such a device.

The semiconductor device may include a silicon body, in which are formed source and drain regions defining between them a channel region, a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer, a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer. The thin silicon layer may have an area greater than that of the gate dielectric layer so that its upper surface includes two opposed zones which extend beyond the gate dielectric layer, the source and drain regions each overlapping respectively, at least in part, one of said opposed zones.

In an embodiment, the buried dielectric layer extends between the source and drain regions.

In another embodiment, the buried dielectric layer extends over the entire surface of the silicon body under the source and drain regions.

Furthermore, the device may be a device of planar structure, in which the surfaces of the source and drain regions and of the gate region on which the contacts are made, lie in the same plane.

In general, the buried dielectric layer has a thickness of 1 to 50 nm, for example around 10 nm.

When the source and drain regions include extensions adjacent to the thin gate dielectric layer (for example SiO_2, Ta_2O_5, Si_3N_4, Al_2O_3, etc.), the buried dielectric layer may lie below these extensions and may be adjacent to these extensions.

The buried dielectric layer may include any appropriate solid or gaseous dielectric, but may be an air-filled cavity.

The thin silicon layer forming the channel of the device has in general a thickness of 1 to 50 nm.

Contact with the thin silicon layer is obtained by removing the second spacers. The exposed zones of the silicon layer therefore allow the (selective) epitaxy of the source and drain regions to be started. The length of each of the exposed zones of the thin silicon layer is equal to the thickness of each of the second spacers, generally ≤ 100 nm.

Another embodiment relates to a process for fabricating the semiconductor device.

The process may include:

the formation of a germanium or SiGe alloy layer on a main surface of a silicon body;

the formation of a thin silicon layer on the germanium or SiGe layer;

the formation of a thin gate dielectric layer on the thin silicon layer;

the formation on the thin gate dielectric layer of a gate having an upper surface coated with a hard mask;

the formation of first spacers made of a first material on two opposed sides of the gate and of the hard mask;

the formation along the first spacers of second spacers made of a second material different from the first material;

the etching, on each side of the second spacers, of the thin gate dielectric layer, of the thin silicon layer and optionally of part of the germanium or SiGe alloy layer;

the selective lateral etching of the germanium or SiGe alloy layer in order to form a tunnel;

optionally, the filling of the tunnel with a solid dielectric;

the removal of the second spacers in order to expose two zones on the thin silicon layer which are located respectively on either side of the first spacers; and

the formation on either side of the first spacers of source and drain regions overlapping, at least in part, said zones.

In one embodiment, the formation of the source and drain regions includes the selective epitaxy of silicon in order to form on either side of the first spacers polycrystalline silicon deposits (which overlap, at least in part, the exposed zones of the thin silicon layer and are precursors of the future source and drain regions), the removal of the gate hard mask and the implantation of a dopant in the polycrystalline silicon deposits in order to produce the source and drain regions.

In another embodiment, the formation of the source and drain regions includes the deposition of a thick polycrystalline silicon encapsulating layer, the formation of a resin mask on the thick polycrystalline silicon layer, the etching of the thick layer, the removal of the mask, the chemical-mechanical polishing of the thick polycrystalline silicon layer down to level with the gate in order to produce parts (which are intended to form the future source and drain regions co-planar with the gate), and the implantation of a dopant in these remaining parts of the thick polycrystalline silicon layer in order to form source and drain regions covering the exposed zones of the thin silicon layer.

In certain embodiments, the process includes, before the step of forming the first spacers, a dopant implantation step in order to form extensions of the source and drain regions and, after the first spacers have been formed, a dopant implantation step (overdoping of the source and drain regions).

SiGe alloys are well known and mention may be made of $Si_{1-x}Ge_x$ alloys in which $0 < x < 1$ and $Si_{1-x-y}Ge_xC_y$ alloys in which $0 < x \leq 0.95$ and $0 < y \leq 0.05$.

In an embodiment, the SiGe alloys have a relatively high germanium content ($x \geq 0.1$ or $0.1 \leq x \leq 0.3$) for better etching selectivity with respect to silicon and to SiO_2.

The selective removal of the germanium or of the SiGe alloy may take place by any known means, for example by means of an oxidizing chemistry such as a solution consisting of 40 ml of 70% HNO_3 + 20 ml of H_2O_2 + 5 ml of 0.5% HF, or by isotropic plasma etching.

BRIEF DESCRIPTION OF THE DRAWINGS

The rest of the description refers to the appended figures which show respectively:

Figure 1, a schematic sectional view of an embodiment of an SON-MOSFET having conventional source and drain regions;

Figure 2, a schematic sectional view of an embodiment of an SON-MOSFET;

Figure 3, a schematic sectional view of another embodiment of an SON-MOSFET;

Figures 4a to 4i, schematic sectional views of the main steps of a method of implementing the process for fabricating a SON-MOSFET; and

Figures 5a to 5i, schematic sectional views of the main steps of another method of implementation.

DETAILED DESCRIPTION OF THE INVENTION

Although the description will be given for a field-effect MOS transistor (SON-MOSFET), it may apply to any other appropriate semiconductor device.

Figure 2 shows a first embodiment of an SON-MOSFET, which includes, as is conventional, a silicon body 10 having an upper surface and source and drain regions 23, 24 defining a channel region between them. As is also conventional, the source and drain regions, 23, 24 include extensions 13' located in the channel region. The upper surface of the body 10 is coated with a thin layer 14 of a gate dielectric, for example SiO_2, and a polycrystalline silicon gate 15 is formed above the channel region and is flanked by spacers 17, 18 made, for example, of Si_3N_4 or SiO_2. Finally, the structure is coated with an encapsulating material 26 and contacts 25 are provided on the source and drain regions 23, 24 and the gate 15.

The structure which has just been described is a conventional MOSFET structure.

In the case of the SON-MOSFET, an air-filled cavity or a layer 22 of an appropriate solid dielectric bridges the source and drain regions 23, 24 beneath the gate 15 so as to isolate a thin silicon layer 13 from the rest of the silicon body 10. This thin silicon layer 13 constitutes the channel of the transistor.

The thin silicon layer 13 generally has a thickness of 1 to 50 nm.

The thickness of the air-filled cavity or of the solid dielectric layer 22 is from 1 to 50 nm or, for example, around 10 nm.

In an embodiment, the thin silicon layer 13 constituting the channel has an area greater than the gate dielectric layer 14, so that its upper surface has two exposed zones 13a extending beyond the gate dielectric layer 14 on either side of the spacers 17, 18.

Also, the source and drain regions 23, 24 may include extensions 23a, 24a each covering respectively, at least in part, one of the two exposed zones 13a of the thin silicon layer 13.

Thus, even with extremely small thicknesses of the thin silicon layer 13, a reliable and sufficient contact is made between the source and drain regions 23, 24 and the thin silicon layer 13 constituting the channel, which may not be the case with a simple lateral contact.

Figure 3 shows another embodiment of an SON-MOSFET having a planar structure, that is to say that the upper surfaces of the source and drain regions and of the gate, on which surfaces the contacts are made, lie in the same plane.

This device differs from the device in Figure 2, apart from the planarization, only by the fact that the buried dielectric layer 22 extends over the entire surface of the silicon body 10, immediately below the source and drain regions 23, 24.

A first method of implementing a process in order to fabricate an SON-MOSFET, like the one shown in Figure 2, will now be described in conjunction with Figures 4a to 4i.

As shown in Figure 4a, the process starts with the successive deposition, by epitaxy (for example by chemical vapor deposition), on a silicon substrate 10, of a germanium or SiGe alloy layer 12, generally having a thickness of between 1 and 50 nm, and a thin silicon layer 13 having a thickness of 1 to 50 nm.

Next, a conventional process is used to form, as shown in Figure 4b, a gate oxide (SiO_2) layer 14 and then a polycrystalline silicon gate 15 on this gate oxide layer 14.

Lightly doped zones 13' may then optionally be formed, by conventional ion implantation, in the thin silicon layer 13, which zones will subsequently serve to form the extensions of the source and drain regions.

As shown in Figure 4b, the upper surface of the gate 15 may be protected by a hard mask 16, for example a silicon oxynitride layer, as is well known, and first spacers 17, 18 made of Si_3N_4 are formed in a known manner on the opposed side walls of the gate 15 and of the hard mask 16.

Second spacers 19, 20 made of SiO_2 are then formed in a conventional manner along the first spacers 17, 18, as shown in Figure 4c.

The gate oxide layer 14, the thin silicon layer 13 and, optionally, an upper part of the Ge or SiGe alloy layer 12 are then etched, for example by means of a plasma, on each side of the second spacers 19, 20, as shown in Figure 4d.

At this stage, the material of the layer 12 is selectively removed in order to form a tunnel 21, as shown in Figure 4e.

Although this is not necessary, the tunnel 21 may be filled with an appropriate solid dielectric 22.

As shown in Figure 4f, the second spacers 19, 20 and the subjacent parts of the gate oxide layer 14 are then removed in order to expose, on the surface of the thin silicon layer 13, two zones 13a located on either side of the first spacers 17, 18.

As shown in Figure 4f', the dielectric layer 22 is removed on either side of the silicon

layer (deoxidation in the case of a SiO_2 layer) so as to start the epitaxy of the source and drain regions.

The process then continues conventionally, as shown in Figure 4g, with the selective deposition of silicon (for example by epitaxial growth) on either side of the first spacers 17, 18 of polycrystalline silicon, so as to form polycrystalline silicon deposits 23, 24. Polycrystalline silicon deposits 23, 24 are precursors of the future source and drain regions, each comprising an extension 23a, 24a respectively overlapping one of the exposed zones 13a of the surface of the thin silicon layer 13.

After the gate hard mask 16 has been removed, a dopant is implanted into the polycrystalline silicon deposits 23, 24 and in the gate 15 (Figure 4h).

The completion of the device, such as the formation of contacts 25 and the possible encapsulation 26, takes place in a completely conventional manner (Figure 4i).

Figures 5a to 5i show a second method of implementing a process, making it possible to obtain a MOSFET with a planar structure as shown in Figure 3.

The steps of the process up to the removal of the Ge or SiGe alloy layer, which are shown in Figures 5a to 5e, are identical to those described in connection with Figures 4a to 4e, apart from the fact that the material constituting the first spacers 17, 18 is SiO_2 and that of the second spacers 19, 20 is Si_3N_4.

After the tunnel 21 has been formed, a dielectric layer 22 is deposited, this layer filling the tunnel and covering the junctions of the main surface of the substrate where subsequently the source and drain regions will be formed (Figure 5f).

As shown in Figure 5g, the entire structure is covered with a thick polycrystalline silicon layer 27 and then with a resin mask 28. The thick polycrystalline silicon layer 27 is then conventionally etched by means of the resin mask to the desired dimensions and geometry.

Figure 5g shows the lateral isolation 11 so as to provide a reference for the etching of the polycrystalline silicon layer 27. For the sake of simplification, this isolation 11 has

not been shown in the other figures.

After the resin mask 28 has been removed, a conventional chemical-mechanical polishing step is then carried out on the thick polycrystalline silicon layer 27 until the gate hard mask 16 has been completely removed. This produces polycrystalline silicon regions 23, 24 intended to form the future source and drain regions having extensions 23a, 24a, which cover the exposed zones 13a of the thin silicon layer 13. A conventional dopant implantation operation is then carried out in order to produce the source and drain regions and the gate.

The structure obtained is a planar structure, that is to say the upper surfaces of the regions 23, 24 and of the gate 15 lie in the same plane.

As shown in Figure 5i, the device is completed as previously by the conventional formation of contacts 25 and of an encapsulation 26.

The devices, in particular the planar devices, the structure of which is similar to that of the SOI devices fabricated using a silicon-on-insulator substrate and their fabrication processes, have many advantages over these SOI devices.

Firstly, the devices may not require the use of an expensive SOI substrate, which usually requires a step of reducing the thickness of the silicon.

The silicon layer in certain embodiments, being formed by epitaxy, may have an arbitrarily small thickness.

Some embodiments allow very small thicknesses of the buried layer of dielectric (or solid material) of the order of a few nanometres, compared with hundreds of nanometres in the case of conventional SOI substrates, this having an advantage from the point of view of eliminating short-channel effects.

Better thermal contact between the channel and the substrate is achieved, thanks to the buried dielectric layer and also because of the fact that this layer does not extend beyond the gate zone.

The link between the thickness of the thin silicon layer and the depth of the junctions is eliminated, thus reducing the series resistances.

It is also possible, by re-oxidizing the rear face of the thin silicon layer constituting the channel (after the Ge or SiGe layer has been removed) to obtain a very good channel/insulator surface finish.

Finally, the problems of etching selectivity of Si with respect to SiO_2 which, in a conventional SOI substrate, may result in the thin oxide layer under the source and drain regions being punctured, are eliminated.

In the Abstract:

An embodiment concerns a semiconductor device having a silicon body in which are formed source and drain regions that define between them a channel region, a thin gate dielectric layer, a buried layer of dielectric material extending between the source and drain regions, and a thin silicon layer extending between the source and drain regions and included between the buried dielectric material layer and the gate dielectric layer. The thin silicon layer may have an area greater than that of the gate dielectric layer such that its upper surface includes two opposite zones extending beyond the gate dielectric layer and the source and drain regions. The source and drain regions may each respectively overlap, at least partly, one of the two opposite zones.

Marked-Up Version of Amendments to Specification, Claims, and Abstract

In the Specification:

~~**Semiconductor device combining the advantages of bulk and SOI architectures, and fabrication process**~~

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates in general to high-performance CMOS semiconductor devices for the rapid processing of signals and/or for low voltage/low-power applications, and more particularly to field-effect MOS transistors (MOSFETs). The novel architecture called "silicon-on-nothing" (SON) architecture combines the advantages of bulk and silicon-on-insulator (SOI) architectures.

2. Description of the Related Art

One of the limiting factors of conventional bulk-architecture MOSFETs is the substrate effect which impairs the properties of the transistor. This drawback is avoided in MOSFETs of silicon-on-insulator (SOI) architecture by separating the thin silicon film from the substrate by a buried silicon oxide layer.

Elimination of the substrate effect in MOSFETs of fully-depleted thin SOI film architecture may results in an increase in the drain current.

However, MOSFETs of ultra-thin SOI architecture suffer from a high source/drain (S/D) resistance because of shallow junctions limited by the thickness of the silicon layer and because of poor thermal conductivity. Furthermore, the cost of fabricating substrates of SOI architecture is high, which has limited their introduction on to the market.

SUMMARY OF THE INVENTION

To remedy the drawbacks of the devices of the prior art, a semiconductor device like

that shown in ~~figure~~Figure 1 has been proposed~~,~~. ~~this~~ This device includes~~comprising~~ a silicon substrate 10, in which are formed source 23 and drain 24 regions, a thin gate dielectric layer 14 on the channel region and a gate 15 on the thin gate dielectric layer 14, a buried layer 22 of a dielectric extending between the source and drain regions and a thin silicon layer 13 lying between the buried dielectric layer 22 and the gate dielectric layer 14, constituting the channel region of the device between the source and drain regions 23, 24. The buried dielectric layer 22 may consist of an air-filled cavity.

Because of the very small thickness of the thin silicon layer 13 constituting the channel, lateral contact of the source 23 and drain 24 regions with this silicon layer 13 is difficult to achieve.

~~The object of the invention is therefore to~~ An embodiment includes modifying the architecture of the junctions of the device described above, so as to make a reliable and easily producible contact between the thin silicon layer constituting the channel and the source and drain regions.

~~The subject of the invention is~~An embodiment also includes a process for producing such a device.

The semiconductor device ~~according to the invention comprises~~includes a silicon body, in which are formed source and drain regions defining between them a channel region, a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer, a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer~~,~~. ~~the~~ The thin silicon layer may ~~having~~ have an area greater than that of the gate dielectric layer so that its upper surface ~~comprise~~includes two opposed zones which extend beyond the gate dielectric layer, the source and drain regions each overlapping respectively, at least in part, one of said opposed zones.

In ~~a first~~an embodiment ~~of the invention~~, the buried dielectric layer extends between the source and drain regions.

In another embodiment ~~of the invention~~, the buried dielectric layer extends over the entire surface of the silicon body under the source and drain regions.

Furthermore, the device may be a device of planar structure, in which the surfaces of the source and drain regions and of the gate region on which the contacts are made, lie in the same plane.

In general, the buried dielectric layer has a thickness of 1 to 50 nm, for example around 10 nm.

When the source and drain regions ~~comprise~~include extensions adjacent to the thin gate dielectric layer (for example SiO_2, Ta_2O_5, Si_3N_4, Al_2O_3, etc.), the buried dielectric layer ~~preferably~~ may lies below these extensions and ~~even more preferably is~~may be adjacent to these extensions.

The buried dielectric layer may ~~consist of~~include any appropriate solid or gaseous dielectric, but ~~it is preferably~~may be an air-filled cavity.

The thin silicon layer forming the channel of the device has in general a thickness of 1 to 50 nm.

Contact with the thin silicon layer is obtained by removing the second spacers~~.~~. The exposed zones of the silicon layer therefore allow the (selective) epitaxy of the source and drain regions to be started~~.~~. The length of each of the exposed zones of the thin silicon layer is equal to the thickness of each of the second spacers, generally ≤ 100 nm.

~~The invention also~~Another embodiment relates to a process for fabricating the semiconductor device ~~according to the invention~~.

The process ~~of the invention comprises~~may include:

~~(a)~~ the formation of a germanium or SiGe alloy layer on a main surface of a silicon body;

~~(b)~~ the formation of a thin silicon layer on the germanium or SiGe layer;

~~(c)~~ the formation of a thin gate dielectric layer on the thin silicon layer;

~~(d)~~ the formation on the thin gate dielectric layer of a gate having an upper surface coated with a hard mask;

~~(e)~~ the formation of first spacers made of a first material on two opposed sides of the gate and of the hard mask;

~~(f)~~ the formation along the first spacers of second spacers made of a second material different from the first material;

~~(g)~~ the etching, on each side of the second spacers, of the thin gate dielectric layer, of the thin silicon layer and optionally of part of the germanium or SiGe alloy layer;

~~(h)~~ the selective lateral etching of the germanium or SiGe alloy layer in order to form a tunnel;

~~(i)~~ optionally, the filling of the tunnel with a solid dielectric;

~~(j)~~ the removal of the second spacers in order to expose two zones on the thin silicon layer which are located respectively on either side of the first spacers; and

~~(k)~~ the formation on either side of the first spacers of source and drain regions overlapping, at least in part, said zones.

In ~~a first method of implementing the invention~~one embodiment, the formation of the source and drain regions ~~comprise~~includes the selective epitaxy of silicon in order to form on either side of the first spacers polycrystalline silicon deposits (which overlap, at least in part, the exposed zones of the thin silicon layer ~~which~~ and are precursors of the future source and drain regions) ~~and which overlap, at least in part, the exposed zones of the thin silicon layer~~, the removal of the gate hard mask and the implantation of a dopant in the polycrystalline silicon deposits in order to produce the source and drain regions.

In ~~a second method of implementing the invention~~another embodiment, the formation of the source and drain regions ~~comprise~~includes the deposition of a thick polycrystalline silicon encapsulating layer, the formation of a resin mask on the thick polycrystalline silicon layer, the etching of the thick layer, the removal of the mask, the chemical-mechanical polishing of the thick polycrystalline silicon layer down to level with the gate in order to produce parts (which are intended to form the future source and drain regions co-planar with the gate), and the implantation of a dopant in these remaining parts of the thick polycrystalline silicon layer in order to form source and drain regions covering the exposed zones of the thin silicon layer.

~~Preferably~~In certain embodiments, the process ~~of the invention~~ includes, before the

step of forming the first spacers, a dopant implantation step in order to form extensions of the source and drain regions and, after the first spacers have been formed, a dopant implantation step (overdoping of the source and drain regions).

SiGe alloys are well known and mention may be made of $Si_{1-x}Ge_x$ alloys in which $0 < x < 1$ and $Si_{1-x-y}Ge_xC_y$ alloys in which $0 < x \leq 0.95$ and $0 < y \leq 0.05$.

~~Preferably~~In an embodiment, the SiGe alloys have a relatively high germanium content ($x \geq 0.1$~~, preferably~~ or $0.1 \leq x \leq 0.3$) for better etching selectivity with respect to silicon and to SiO_2.

The selective removal of the germanium or of the SiGe alloy may take place by any known means, for example by means of an oxidizing chemistry such as a solution consisting of 40 ml of 70% HNO_3 + 20 ml of H_2O_2 + 5 ml of 0.5% HF, or by isotropic plasma etching.

BRIEF DESCRIPTION OF THE DRAWINGS

The rest of the description refers to the appended figures which show respectively:

~~— figure~~ Figure 1, a schematic sectional view of an embodiment of an SON-MOSFET having conventional source and drain regions;

~~— figure~~ Figure 2, a schematic sectional view of an embodiment of an SON-MOSFET ~~according to the invention~~;

~~— f~~Figure 3, a schematic sectional view of another embodiment of an SON-MOSFET ~~according to the invention~~;

~~— f~~Figures 4a to 4i, schematic sectional views of the main steps of a ~~first~~ method of implementing the process for fabricating a SON-MOSFET ~~according to the invention~~; and

~~— f~~Figures 5a to 5i, schematic sectional views of the main steps of ~~a second~~another method of implementation.

DETAILED DESCRIPTION OF THE INVENTION

Although the description will be given for a field-effect MOS transistor ~~according to the invention~~ (SON-MOSFET), it may apply to any other appropriate semiconductor

device.

Figure 2 shows a first embodiment of an SON-MOSFET ~~according to the invention~~, which ~~comprises~~includes, as is conventional, a silicon body 10 having an upper surface and source and drain regions 23, 24 defining a channel region between them~~.~~. As is also conventional, the source and drain regions, 23, 24 include extensions 13' located in the channel region~~.~~. The upper surface of the body 10 is coated with a thin layer 14 of a gate dielectric, for example SiO_2, and a polycrystalline silicon gate 15 is formed above the channel region and is flanked by spacers 17, 18 made, for example, of Si_3N_4 or SiO_2~~.~~. Finally, the structure is coated with an encapsulating material 26 and contacts 25 are provided on the source and drain regions 23, 24 and the gate 15.

The structure which has just been described is a conventional MOSFET structure.

In the case of the SON-MOSFET, an air-filled cavity or a layer 22 of an appropriate solid dielectric bridges the source and drain regions 23, 24 beneath the gate 15 so as to isolate a thin silicon layer 13 from the rest of the silicon body 10. This thin silicon layer 13 constitutes the channel of the transistor.

The thin silicon layer 13 generally has a thickness of 1 to 50 nm.

The thickness of the air-filled cavity or of the solid dielectric layer 22 is from 1 to 50 nm ~~, preferably~~or, for example, around 10 nm.

~~According to the invention~~In an embodiment, the thin silicon layer 13 constituting the channel has an area greater than the gate dielectric layer 14, so that its upper surface has two exposed zones 13a extending beyond the gate dielectric layer 14 on either side of the spacers 17, 18.

Also ~~according to the invention~~, the source and drain regions 23, 24 may include extensions 23a, 24a each covering respectively, at least in part, one of the two exposed zones 13a of the thin silicon layer 13.

Thus, even with extremely small thicknesses of the thin silicon layer 13, a reliable and sufficient contact is made between the source and drain regions 23, 24 and the thin

silicon layer 13 constituting the channel, which ~~could~~ may not be the case with a simple lateral contact.

Figure 3 shows another embodiment of an SON-MOSFET ~~according to the invention~~ having a planar structure, that is to say that the upper surfaces of the source and drain regions and of the gate, on which surfaces the contacts are made, lie in the same plane.

This device differs from the device in ~~figure~~Figure 2, apart from the planarization, only by the fact that the buried dielectric layer 22 extends over the entire surface of the silicon body 10, immediately below the source and drain regions 23, 24.

A first method of implementing ~~the~~ a process ~~of the invention~~ in order to fabricate an SON-MOSFET, like the one shown in ~~figure~~Figure 2, will now be described in conjunction with ~~figure~~Figures 4a to 4i.

As shown in ~~figure~~Figure 4a, the process starts with the successive deposition, by epitaxy (for example by chemical vapor deposition), on a silicon substrate 10, of a germanium or SiGe alloy layer 12, generally having a thickness of between 1 and 50 nm, and a thin silicon layer 13 having a thickness of 1 to 50 nm.

Next, a conventional process is used to form, as shown in ~~figure~~Figure 4b, a gate oxide (SiO_2) layer 14 and then a polycrystalline silicon gate 15 on this gate oxide layer 14.

Lightly doped zones 13' may then optionally be formed, by conventional ion implantation, in the thin silicon layer ~~17~~13, which zones will subsequently serve to form the extensions of the source and drain regions.

As shown in ~~figure~~Figure 4b, the upper surface of the gate 15 may be protected by a hard mask 16, for example a silicon oxynitride layer, as is well known, and first spacers 17, 18 made of Si_3N_4 are formed in a known manner on the opposed side walls of the gate 15 and of the hard mask 16.

Second spacers 19, 20 made of SiO_2 are then formed in a conventional manner along the first spacers 17, 18, as shown in ~~figure~~Figure 4c.

The gate oxide layer 14, the thin silicon layer 13 and, optionally, an upper part of the Ge or SiGe alloy layer 12 are then etched, for example by means of a plasma, on each side of the second spacers 19, 20, as shown in ~~figure~~Figure 4d.

At this stage, the material of the layer 12 is selectively removed in order to form a tunnel 21, as shown in ~~figure~~Figure 4e.

Although this is not necessary, the tunnel 21 may be filled with an appropriate solid dielectric 22.

As shown in ~~figure~~Figure 4f, the second spacers 19, 20 and the subjacent parts of the gate oxide layer 14 are then removed in order to expose, on the surface of the thin silicon layer 13, two zones 13a located on either side of the first spacers 17, 18.

As shown in ~~figure~~Figure 4f', the dielectric layer 22 is removed on either side of the silicon layer (deoxidation in the case of a SiO_2 layer) so as to start the epitaxy of the source and drain regions.

The process then continues conventionally, as shown in ~~figure~~Figure 4g, with the selective deposition of silicon (for example by epitaxial growth) on either side of the first spacers 17, 18 of polycrystalline silicon, so as to form polycrystalline silicon deposits 23, 24. Polycrystalline silicon deposits 23, 24 ~~which~~ are precursors of the future source and drain regions, each comprising an extension 23a, 24a respectively overlapping one of the exposed zones 13a of the surface of the thin silicon layer 13.

After the gate hard mask 16 has been removed, a dopant is implanted into the polycrystalline silicon deposits 23, 24 and in the gate 15 (~~figure~~Figure 4h).

The completion of the device, such as the formation of contacts 25 and the possible encapsulation 26, takes place in a completely conventional manner (~~figure~~Figure 4i).

Figures 5a to 5i show a second method of implementing ~~the~~ a process ~~of the invention~~, making it possible to obtain a MOSFET ~~according to the invention~~ with a planar structure as shown in ~~figure~~Figure 3.

The steps of the process up to the removal of the Ge or SiGe alloy layer, which are shown in ~~figure~~Figures 5a to 5e, are identical to those described in connection with ~~figure~~Figures 4a to 4e, apart from the fact that the material constituting the first spacers 17, 18 is SiO_2 and that of the second spacers 19, 20 is Si_3N_4.

After the tunnel 21 has been formed, a dielectric layer 22 is deposited, this layer filling the tunnel and covering the junctions of the main surface of the substrate where subsequently the source and drain regions will be formed (~~figure~~Figure 5f).

As shown in ~~figure~~Figure 5g, the entire structure is covered with a thick polycrystalline silicon layer 27 and then with a resin mask 28. The thick polycrystalline silicon layer 27 is then conventionally etched by means of the resin mask to the desired dimensions and geometry.

Figure 5g shows the lateral isolation 11 so as to provide a reference for the etching of the polycrystalline silicon layer 27. For the sake of simplification, this isolation 11 has not been shown in the other figures.

After the resin mask 28 has been removed, a conventional chemical-mechanical polishing step is then carried out on the thick polycrystalline silicon layer 27~~,~~ until the gate hard mask 16 has been completely removed.~~, so as to~~This produces polycrystalline silicon regions 23, 24 intended to form the future source and drain regions having extensions 23a, 24a, which cover the exposed zones 13a of the thin silicon layer 13. A conventional dopant implantation operation is then carried out in order to produce the source and drain regions and the gate.

The structure obtained is a planar structure, that is to say the upper surfaces of the regions 23, 24 and of the gate 15 lie in the same plane.

As shown in ~~figure~~Figure 5i, the device is completed as previously by the conventional formation of contacts 25 and of an encapsulation 26.

The devices, in particular the planar devices, ~~according to the invention,~~ the structure of which is similar to that of the SOI devices fabricated using a silicon-on-insulator

substrate~~,~~ and their fabrication processes, have many advantages over these SOI devices.

Firstly, ~~they do~~the devices may not require the use of an expensive SOI substrate, which usually requires a step of reducing the thickness of the silicon.

The silicon layer in ~~the processes of the invention~~certain embodiments, being formed by epitaxy, may have an arbitrarily small thickness.

~~The process of the invention~~Some embodiments allows very small thicknesses of the buried layer of dielectric (or solid material) of the order of a few nanometres, compared with hundreds of nanometres in the case of conventional SOI substrates, this having an advantage from the point of view of eliminating short-channel effects.

Better thermal contact between the channel and the substrate is achieved, thanks to the buried dielectric layer and also because of the fact that this layer does not extend beyond the gate zone.

The link between the thickness of the thin silicon layer and the depth of the junctions is eliminated, thus reducing the series resistances.

It is also possible, by re-oxidizing the rear face of the thin silicon layer constituting the channel (after the Ge or SiGe layer has been removed) to obtain a very good channel/insulator surface finish.

Finally, the problems of etching selectivity of Si with respect to SiO_2 which, in a conventional SOI substrate, may result in the thin oxide layer under the source and drain regions being punctured, are eliminated.

In the Claims:

1. (Amended) A semiconductor device, comprising:

-a silicon body ~~(10)~~, in which are formed source and drain regions ~~(23, 24)~~ defining between them a channel region~~,~~;

a thin gate dielectric layer ~~(14)~~ on the channel region and a gate ~~(15)~~ on the thin gate dielectric layer~~,~~; and

a buried layer ~~(22)~~ of a dielectric and a thin silicon layer ~~(13)~~ extending between the source and drain regions and lying between the buried dielectric layer ~~(22)~~ and the gate dielectric layer ~~(14)~~, ~~characterized in that this~~wherein the thin silicon layer ~~(13)~~ has an area greater than that of the gate dielectric layer ~~(14)~~ so that its upper surface comprises two opposed zones ~~(13a)~~ which extend beyond the gate dielectric layer ~~(14)~~ and in that the source and drain regions ~~(23, 24)~~ each overlap respectively, at least in part, one of said opposed zones ~~(13a)~~.

2. (Amended) The device ~~as claimed in~~of claim 1, ~~characterized in that~~wherein the buried dielectric layer ~~(22)~~ extends between the source and drain regions ~~(23, 24)~~.

3. (Amended) The device ~~as claimed in~~of claim 1, ~~characterized in that~~wherein the buried dielectric layer ~~(22)~~ extends over the entire surface of the silicon body ~~(10)~~ below the source and drain regions ~~(23, 24)~~.

4. (Amended) The device ~~as claimed in any one of claims 1 to 3~~of claim 1, ~~characterized in that it~~wherein the device has a planar structure.

5. (Amended) The device ~~as claimed in any one of claims 1 to 4~~of claim 1, ~~characterized in that~~wherein the buried dielectric layer ~~(22)~~ is an air-filled cavity.

6. (Amended) The device ~~as claimed in any one of claims 1 to 4~~of claim 1, ~~characterized in that~~wherein the buried dielectric layer ~~(22)~~ is a solid material.

7. (Amended) The device ~~as claimed in any one of claims 1 to 6~~of claim 1,

~~characterized in that~~wherein the device is a transistor.

8. (Amended) ~~A process for fabricating a device as claimed in claim 1, characterized in that it comprises~~comprising:

~~(a) the~~ formation~~ng of~~ a germanium or SiGe alloy layer ~~(12)~~ on a main surface of a silicon body ~~(10)~~;

~~(b) the~~ formation~~ng of~~ a thin silicon layer ~~(13)~~ on the germanium or SiGe alloy layer ~~(12)~~;

~~(c)~~ forming ~~the formation of~~ a thin gate dielectric layer ~~(14)~~ on the thin silicon layer ~~(13)~~;

~~(d)~~ forming a gate ~~the formation~~ on the gate dielectric layer ~~(14) of a gate (15)~~ and ~~of the~~ a hard mask ~~(16)~~ on the gate;

~~(e)~~ forming ~~the formation of~~ first spacers ~~(17, 18) made of a first material~~ on two opposed sides of the gate ~~(15)~~ and of the hard mask, wherein the first spacers are made of a first material ~~(16)~~;

~~(f)~~ forming second spacers ~~the formation~~ along the first spacers, wherein the second spacers are ~~(17, 18) of second spacers (19, 20)~~ made of a second material different from the first material;

~~(g) the~~ etching, on each side of the second spacers ~~(19, 20)~~, of the gate dielectric layer ~~(14)~~, of the thin silicon layer, ~~(13)~~ and optionally of part of the germanium or SiGe alloy layer ~~(12)~~;

~~(h) the~~ selective etching of the germanium or SiGe alloy layer ~~(12)~~ in order to form a tunnel ~~(21)~~;

~~(i)~~ optionally, ~~the~~ filling ~~of~~ the tunnel ~~(21)~~ with a solid dielectric ~~(22)~~;

~~(j) the~~ removal~~ing of~~ the second spacers ~~(19, 20)~~ in order to expose two zones ~~(13a)~~ on the thin silicon layer, wherein the two zones ~~(13) which~~ are located respectively on either side of the first spacers ~~(17, 18)~~; and

~~(k)~~ forming source and drain regions ~~the formation~~ on either side of the first spacers, wherein the source and drain regions ~~(17, 18) of source and drain regions (23, 24; 23a, 24a)~~ overlapping, at least in part, ~~said~~ the two zones ~~(13a)~~.

9. (Amended) The process ~~as claimed in~~of claim 8, ~~characterized in that~~wherein forming ~~the formation of~~ the source and drain regions ~~(23, 24)~~ comprises ~~the~~ deposition of polycrystalline silicon by selective epitaxy in order to form polycrystalline silicon deposits on either side of the first spacers, wherein the

polycrystalline silicon deposits ~~(17, 18) polycrystalline silicon deposits which~~ are precursors of the ~~future~~ source and drain regions and ~~which~~ overlap, at least in part, the exposed zones ~~(13a)~~ of the thin silicon layer ~~(13)~~, and the method further comprising ~~removal~~ removing ~~of~~ the gate hard mask ~~16~~ and ~~the~~ implantation~~ng~~ ~~of~~ a dopant in the polycrystalline silicon deposits in order to produce the source and drain regions.

10. (Amended) The process ~~as claimed in~~of claim 8, ~~characterized in that~~wherein forming ~~the formation of~~ the source and drain regions comprises ~~the~~ deposition of a thick polycrystalline silicon encapsulating layer ~~(27)~~, forming ~~the formation of~~ a resin mask ~~(28)~~ on the thick polycrystalline silicon layer ~~(27)~~, ~~the~~ etching of the thick polycrystalline silicon layer to the desired shape and dimensions ~~(27)~~ by means of the resin mask ~~to the desired shape and dimensions~~, ~~the removal~~removing of the resin mask ~~(28)~~, ~~the~~ chemical-mechanical polishing of the thick silicon layer ~~(23)~~ down to level with the gate ~~(15)~~ in order to produce parts ~~(23, 24)~~ in the thick polycrystalline silicon layer ~~(23)~~ which are intended to form ~~future~~ the source and drain regions co-planar with the gate and ~~the~~ implantation~~ing~~ of a dopant in ~~said~~ the parts ~~(23, 24)~~ in order to form the source and drain regions.

In the Abstract:

~~The invention~~An embodiment concerns a semiconductor device ~~comprises~~ having a silicon body ~~(10) wherein~~in which are formed source and drain regions that ~~(23, 24) defining~~ define between them a channel region, a thin gate dielectric layer, a buried layer of dielectric material ~~(22)~~ extending between the source and drain regions, ~~(23, 24)~~ and a thin silicon layer ~~(13)~~ extending between the source and drain regions and included between the buried dielectric material layer ~~(22)~~ and the gate dielectric layer ~~(14)~~. The ~~invention is characterised in that said~~ thin silicon layer ~~(13) has~~may have an area greater than that of the gate dielectric layer ~~(4)~~ such that its upper surface ~~comprises~~ includes two opposite zones ~~(13)~~ extending beyond the gate dielectric layer ~~(4)~~ and the source and drain regions. The source and drain regions may ~~(8, 9)~~ each respectively overlapping, at least partly, one of ~~said~~ the two opposite zones ~~(13a)~~. ~~The invention is appicable to transistors.~~

that shown in ~~figure~~Figure 1 has been proposed~~,~~. ~~this~~ This device includes~~comprising~~ a silicon substrate 10, in which are formed source 23 and drain 24 regions, a thin gate dielectric layer 14 on the channel region and a gate 15 on the thin gate dielectric layer 14, a buried layer 22 of a dielectric extending between the source and drain regions and a thin silicon layer 13 lying between the buried dielectric layer 22 and the gate dielectric layer 14, constituting the channel region of the device between the source and drain regions 23, 24. The buried dielectric layer 22 may consist of an air-filled cavity.

Because of the very small thickness of the thin silicon layer 13 constituting the channel, lateral contact of the source 23 and drain 24 regions with this silicon layer 13 is difficult to achieve.

~~The object of the invention is therefore to~~ An embodiment includes modifying the architecture of the junctions of the device described above, so as to make a reliable and easily producible contact between the thin silicon layer constituting the channel and the source and drain regions.

~~The subject of the invention is~~An embodiment also includes a process for producing such a device.

The semiconductor device ~~according to the invention comprises~~may include a silicon body, in which are formed source and drain regions defining between them a channel region, a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer, a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer~~,~~. ~~the~~ The thin silicon layer may ~~having~~ have an area greater than that of the gate dielectric layer so that its upper surface ~~comprise~~includes two opposed zones which extend beyond the gate dielectric layer, the source and drain regions each overlapping respectively, at least in part, one of said opposed zones.

In ~~a first~~an embodiment ~~of the invention~~, the buried dielectric layer extends between the source and drain regions.

In another embodiment ~~of the invention~~, the buried dielectric layer extends over the entire surface of the silicon body under the source and drain regions.

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SEMICONDUCTOR DEVICE COMBINING THE ADVANTAGES OF MASSIVE AND SOI ARCHITECTURE, AND METHOD FOR MAKING SAME

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Semiconductor device combining the advantages of bulk and SOI architectures, and fabrication process

The present invention relates in general to high-performance CMOS semiconductor devices for the rapid processing of signals and/or for low voltage/low-power applications, and more particularly to field-effect MOS transistors (MOSFETs). The novel architecture called "silicon-on-nothing" (SON) architecture combines the advantages of bulk and silicon-on-insulator (SOI) architectures.

One of the limiting factors of conventional bulk-architecture MOSFETs is the substrate effect which impairs the properties of the transistor. This drawback is avoided in MOSFETs of silicon-on-insulator (SOI) architecture by separating the thin silicon film from the substrate by a buried silicon oxide layer.

Elimination of the substrate effect in MOSFETs of fully-depleted thin SOI film architecture results in an increase in the drain current.

However, MOSFETs of ultra-thin SOI architecture suffer from a high source/drain (S/D) resistance because of shallow junctions limited by the thickness of the silicon layer and because of poor thermal conductivity. Furthermore, the cost of fabricating substrates of SOI architecture is high, which has limited their introduction on to the market.

To remedy the drawbacks of the devices of the prior art, a semiconductor device like that shown in figure 1 has been proposed, this device comprising a silicon substrate 10, in which are formed source 23 and drain 24 regions, a thin gate dielectric layer 14 on the channel region and a gate 15 on the thin gate dielectric layer 14, a buried layer 22 of a dielectric extending between the source and drain regions and a thin silicon layer 13 lying between the buried dielectric layer 22 and the gate dielectric layer 14, constituting the channel region of the device between the source and drain regions 23, 24. The buried dielectric layer 22 may consist of an air-filled cavity.

Because of the very small thickness of the thin silicon layer 13 constituting the channel, lateral contact of the source 23 and drain 24 regions with this silicon layer 13

is difficult to achieve.

The object of the invention is therefore to modify the architecture of the junctions of the device described above, so as to make a reliable and easily producible contact between the thin silicon layer constituting the channel and the source and drain regions.

The subject of the invention is also a process for producing such a device.

The semiconductor device according to the invention comprises a silicon body, in which are formed source and drain regions defining between them a channel region, a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer, a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer, the thin silicon layer having an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer, the source and drain regions each overlapping respectively, at least in part, one of said opposed zones.

In a first embodiment of the invention, the buried dielectric layer extends between the source and drain regions.

In another embodiment of the invention, the buried dielectric layer extends over the entire surface of the silicon body under the source and drain regions.

Furthermore, the device may be a device of planar structure, in which the surfaces of the source and drain regions and of the gate region on which the contacts are made, lie in the same plane.

In general, the buried dielectric layer has a thickness of 1 to 50 nm, for example around 10 nm.

When the source and drain regions comprise extensions adjacent to the thin gate dielectric layer (for example SiO_2, Ta_2O_5, Si_3N_4, Al_2O_3, etc.), the buried dielectric layer preferably lies below these extensions and even more preferably is adjacent to

these extensions.

The buried dielectric layer may consist of any appropriate solid or gaseous dielectric, but it is preferably an air-filled cavity.

The thin silicon layer forming the channel of the device has in general a thickness of 1 to 50 nm.

Contact with the thin silicon layer is obtained by removing the second spacers. The exposed zones of the silicon layer therefore allow the (selective) epitaxy of the source and drain regions to be started. The length of each of the exposed zones of the thin silicon layer is equal to the thickness of each of the second spacers, generally ≤ 100 nm.

The invention also relates to a process for fabricating the semiconductor device according to the invention.

The process of the invention comprises:

(a) the formation of a germanium or SiGe alloy layer on a main surface of a silicon body;

(b) the formation of a thin silicon layer on the germanium or SiGe layer;

(c) the formation of a thin gate dielectric layer on the thin silicon layer;

(d) the formation on the thin gate dielectric layer of a gate having an upper surface coated with a hard mask;

(e) the formation of first spacers made of a first material on two opposed sides of the gate and of the hard mask;

(f) the formation along the first spacers of second spacers made of a second material different from the first material;

(g) the etching, on each side of the second spacers, of the thin gate dielectric layer, of the thin silicon layer and optionally of part of the germanium or SiGe alloy layer;

(h) the selective lateral etching of the germanium or SiGe alloy layer in order to form a tunnel;

(i) optionally, the filling of the tunnel with a solid dielectric;

(j) the removal of the second spacers in order to expose two zones on the thin

silicon layer which are located respectively on either side of the first spacers; and

(k) the formation on either side of the first spacers of source and drain regions overlapping, at least in part, said zones.

In a first method of implementing the invention, the formation of the source and drain regions comprises the selective epitaxy of silicon in order to form on either side of the first spacers polycrystalline silicon deposits which are precursors of the future source and drain regions and which overlap, at least in part, the exposed zones of the thin silicon layer, the removal of the gate hard mask and the implantation of a dopant in the polycrystalline silicon deposits in order to produce the source and drain regions.

In a second method of implementing the invention, the formation of the source and drain regions comprises the deposition of a thick polycrystalline silicon encapsulating layer, the formation of a resin mask on the thick polycrystalline silicon layer, the etching of the thick layer, the removal of the mask, the chemical-mechanical polishing of the thick polycrystalline silicon layer down to level with the gate in order to produce parts which are intended to form the future source and drain regions co-planar with the gate and the implantation of a dopant in these remaining parts of the thick polycrystalline silicon layer in order to form source and drain regions covering the exposed zones of the thin silicon layer.

Preferably, the process of the invention includes, before the step of forming the first spacers, a dopant implantation step in order to form extensions of the source and drain regions and, after the first spacers have been formed, a dopant implantation step (overdoping of the source and drain regions).

SiGe alloys are well known and mention may be made of $Si_{1-x}Ge_x$ alloys in which $0 < x < 1$ and $Si_{1-x-y}Ge_xC_y$ alloys in which $0 < x \leq 0.95$ and $0 < y \leq 0.05$.

Preferably, the SiGe alloys have a relatively high germanium content ($x \geq 0.1$, preferably $0.1 \leq x \leq 0.3$) for better etching selectivity with respect to silicon and to SiO_2.

The selective removal of the germanium or of the SiGe alloy may take place by any known means, for example by means of an oxidizing chemistry such as a solution

consisting of 40 ml of 70% HNO_3 + 20 ml of H_2O_2 + 5 ml of 0.5% HF, or by isotropic plasma etching.

The rest of the description refers to the appended figures which show respectively:

- figure 1, a schematic sectional view of an embodiment of an SON-MOSFET having conventional source and drain regions;
- figure 2, a schematic sectional view of an embodiment of an SON-MOSFET according to the invention;
- figure 3, a schematic sectional view of another embodiment of an SON-MOSFET according to the invention;
- figures 4a to 4i, schematic sectional views of the main steps of a first method of implementing the process for fabricating a SON-MOSFET according to the invention; and
- figures 5a to 5i, schematic sectional views of the main steps of a second method of implementation.

Although the description will be given for a field-effect MOS transistor according to the invention (SON-MOSFET), it may apply to any other appropriate semiconductor device.

Figure 2 shows a first embodiment of an SON-MOSFET according to the invention, which comprises, as is conventional, a silicon body 10 having an upper surface and source and drain regions 23, 24 defining a channel region between them. As is also conventional, the source and drain regions, 23, 24 include extensions 13' located in the channel region. The upper surface of the body 10 is coated with a thin layer 14 of a gate dielectric, for example SiO_2, and a polycrystalline silicon gate 15 is formed above the channel region and is flanked by spacers 17, 18 made, for example, of Si_3N_4 or SiO_2. Finally, the structure is coated with an encapsulating material 26 and contacts 25 are provided on the source and drain regions 23, 24 and the gate 15.

The structure which has just been described is a conventional MOSFET structure.

In the case of the SON-MOSFET, an air-filled cavity or a layer 22 of an appropriate solid dielectric bridges the source and drain regions 23, 24 beneath the gate 15 so as to isolate a thin silicon layer 13 from the rest of the silicon body 10. This thin silicon

layer 13 constitutes the channel of the transistor.

The thin silicon layer 13 generally has a thickness of 1 to 50 nm.

The thickness of the air-filled cavity or of the solid dielectric layer 22 is from 1 to 50 nm, preferably around 10 nm.

According to the invention, the thin silicon layer 13 constituting the channel has an area greater than the gate dielectric layer 14, so that its upper surface has two exposed zones 13a extending beyond the gate dielectric layer 14 on either side of the spacers 17, 18.

Also according to the invention, the source and drain regions 23, 24 include extensions 23a, 24a each covering respectively, at least in part, one of the two exposed zones 13a of the thin silicon layer 13.

Thus, even with extremely small thicknesses of the thin silicon layer 13, a reliable and sufficient contact is made between the source and drain regions 23, 24 and the thin silicon layer 13 constituting the channel, which could not be the case with a simple lateral contact.

Figure 3 shows another embodiment of an SON-MOSFET according to the invention having a planar structure, that is to say that the upper surfaces of the source and drain regions and of the gate, on which surfaces the contacts are made, lie in the same plane.

This device differs from the device in figure 2, apart from the planarization, only by the fact that the buried dielectric layer 22 extends over the entire surface of the silicon body 10, immediately below the source and drain regions 23, 24.

A first method of implementing the process of the invention in order to fabricate an SON-MOSFET, like the one shown in figure 2, will now be described in conjunction with figures 4a to 4i.

As shown in figure 4a, the process starts with the successive deposition, by epitaxy (for example by chemical vapor deposition), on a silicon substrate 10, of a germanium

or SiGe alloy layer 12, generally having a thickness of between 1 and 50 nm, and a thin silicon layer 13 having a thickness of 1 to 50 nm.

Next, a conventional process is used to form, as shown in figure 4b, a gate oxide (SiO_2) layer 14 and then a polycrystalline silicon gate 15 on this gate oxide layer 14.

Lightly doped zones 13 may then optionally be formed, by conventional ion implantation, in the thin silicon layer 17, which zones will subsequently serve to form the extensions of the source and drain regions.

As shown in figure 4b, the upper surface of the gate 15 may be protected by a hard mask 16, for example a silicon oxynitride layer, as is well known, and first spacers 17, 18 made of Si_3N_4 are formed in a known manner on the opposed side walls of the gate 15 and of the hard mask 16.

Second spacers 19, 20 made of SiO_2 are then formed in a conventional manner along the first spacers 17, 18, as shown in figure 4c.

The gate oxide layer 14, the thin silicon layer 13 and, optionally, an upper part of the Ge or SiGe alloy layer 12 are then etched, for example by means of a plasma, on each side of the second spacers 19, 20, as shown in figure 4d.

At this stage, the material of the layer 12 is selectively removed in order to form a tunnel 21, as shown in figure 4e.

Although this is not necessary, the tunnel 21 may be filled with an appropriate solid dielectric 22.

As shown in figure 4f, the second spacers 19, 20 and the subjacent parts of the gate oxide layer 14 are then removed in order to expose, on the surface of the thin silicon layer 13, two zones 13a located on either side of the first spacers 17, 18.

As shown in figure 4f', the dielectric layer 22 is removed on either side of the silicon layer (deoxidation in the case of a SiO_2 layer) so as to start the epitaxy of the source and drain regions.

The process then continues conventionally, as shown in figure 4g, with the selective deposition of silicon (for example by epitaxial growth) on either side of the first spacers 17, 18 of polycrystalline silicon, so as to form polycrystalline silicon deposits 23, 24 which are precursors of the future source and drain regions, each comprising an extension 23a, 24a respectively overlapping one of the exposed zones 13a of the surface of the thin silicon layer 13.

After the gate hard mask 16 has been removed, a dopant is implanted into the polycrystalline silicon deposits 23, 24 and in the gate 15 (figure 4h).

The completion of the device, such as the formation of contacts 25 and the possible encapsulation 26, takes place in a completely conventional manner (figure 4i).

Figures 5a to 5i show a second method of implementing the process of the invention, making it possible to obtain a MOSFET according to the invention with a planar structure as shown in figure 3.

The steps of the process up to the removal of the Ge or SiGe alloy layer, which are shown in figures 5a to 5e, are identical to those described in connection with figures 4a to 4e, apart from the fact that the material constituting the first spacers 17, 18 is SiO_2 and that of the second spacers 19, 20 is Si_3N_4.

After the tunnel 21 has been formed, a dielectric layer 22 is deposited, this layer filling the tunnel and covering the junctions of the main surface of the substrate where subsequently the source and drain regions will be formed (figure 5f).

As shown in figure 5g, the entire structure is covered with a thick polycrystalline silicon layer 27 and then with a resin mask 28. The thick polycrystalline silicon layer 27 is then conventionally etched by means of the resin mask to the desired dimensions and geometry.

Figure 5g shows the lateral isolation 11 so as to provide a reference for the etching of the polycrystalline silicon layer 27. For the sake of simplification, this isolation 11 has not been shown in the other figures.

After the resin mask 28 has been removed, a conventional chemical-mechanical polishing step is then carried out on the thick polycrystalline silicon layer 27, until the gate hard mask 16 has been completely removed, so as to produce polycrystalline silicon regions 23, 24 intended to form the future source and drain regions having extensions 23a, 24a, which cover the exposed zones 13a of the thin silicon layer 13. A conventional dopant implantation operation is then carried out in order to produce the source and drain regions and the gate.

The structure obtained is a planar structure, that is to say the upper surfaces of the regions 23, 24 and of the gate 15 lie in the same plane.

As shown in figure 5i, the device is completed as previously by the conventional formation of contacts 25 and of an encapsulation 26.

The devices, in particular the planar devices, according to the invention, the structure of which is similar to that of the SOI devices fabricated using a silicon-on-insulator substrate, and their fabrication processes, have many advantages over these SOI devices.

Firstly, they do not require the use of an expensive SOI substrate, which usually requires a step of reducing the thickness of the silicon.

The silicon layer in the processes of the invention, being formed by epitaxy, may have an arbitrarily small thickness.

The process of the invention allows very small thicknesses of the buried layer of dielectric (or solid material) of the order of a few nanometres, compared with hundreds of nanometres in the case of conventional SOI substrates, this having an advantage from the point of view of eliminating short-channel effects.

Better thermal contact between the channel and the substrate is achieved, thanks to the buried dielectric layer and also because of the fact that this layer does not extend beyond the gate zone.

The link between the thickness of the thin silicon layer and the depth of the junctions is eliminated, thus reducing the series resistances.

It is also possible, by re-oxidizing the rear face of the thin silicon layer constituting the channel (after the Ge or SiGe layer has been removed) to obtain a very good channel/insulator surface finish.

Finally, the problems of etching selectivity of Si with respect to SiO_2 which, in a conventional SOI substrate, may result in the thin oxide layer under the source and drain regions being punctured, are eliminated.

CLAIMS

1. A semiconductor device comprising a silicon body (10), in which are formed source and drain regions (23, 24) defining between them a channel region, a thin gate dielectric layer (14) on the channel region and a gate (15) on the thin gate dielectric layer, a buried layer (22) of a dielectric and a thin silicon layer (13) extending between the source and drain regions and lying between the buried dielectric layer (22) and the gate dielectric layer (14), characterized in that this silicon layer (13) has an area greater than that of the gate dielectric layer (14) so that its upper surface comprises two opposed zones (13a) which extend beyond the gate dielectric layer (14) and in that the source and drain regions (23, 24) each overlap respectively, at least in part, one of said opposed zones (13a).

2. The device as claimed in claim 1, characterized in that the buried dielectric layer (22) extends between the source and drain regions (23, 24).

3. The device as claimed in claim 1, characterized in that the buried dielectric layer (22) extends over the entire surface of the silicon body (10) below the source and drain regions (23, 24).

4. The device as claimed in any one of claims 1 to 3, characterized in that it has a planar structure.

5. The device as claimed in any one of claims 1 to 4, characterized in that the buried dielectric layer (22) is an air-filled cavity.

6. The device as claimed in any one of claims 1 to 4, characterized in that the buried dielectric layer (22) is a solid material.

7. The device as claimed in any one of claims 1 to 6, characterized in that the device is a transistor.

8. A process for fabricating a device as claimed in claim 1, characterized in that it comprises:

(a) the formation of a germanium or SiGe alloy layer (12) on a main surface of

a silicon body (10);

(b) the formation of a thin silicon layer (13) on the germanium or SiGe layer (12);

(c) the formation of a thin gate dielectric layer (14) on the thin silicon layer (13);

(d) the formation on the gate dielectric layer (14) of a gate (15) and of the hard mask (16) on the gate;

(e) the formation of first spacers (17, 18) made of a first material on two opposed sides of the gate (15) and of the hard mask (16);

(f) the formation along the first spacers (17, 18) of second spacers (19, 20) made of a second material different from the first material;

(g) the etching, on each side of the second spacers (19, 20), of the gate dielectric layer (14), of the thin silicon layer (13) and optionally of part of the germanium or SiGe alloy layer (12);

(h) the selective etching of the germanium or SiGe alloy layer (12) in order to form a tunnel (21);

(i) optionally, the filling of the tunnel (21) with a solid dielectric (22);

(j) the removal of the second spacers (19, 20) in order to expose two zones (13a) on the thin silicon layer (13) which are located respectively on either side of the first spacers (17, 18); and

(k) the formation on either side of the first spacers (17, 18) of source and drain regions (23, 24; 23a, 24a) overlapping, at least in part, said zones (13a).

9. The process as claimed in claim 8, characterized in that the formation of the source and drain regions (23, 24) comprises the deposition of polycrystalline silicon by selective epitaxy in order to form on either side of the first spacers (17, 18) polycrystalline silicon deposits which are precursors of the future source and drain regions and which overlap, at least in part, the exposed zones (13a) of the thin silicon layer (13), the removal of the gate hard mask 16 and the implantation of a dopant in the polycrystalline silicon deposits in order to produce the source and drain regions.

10. The process as claimed in claim 8, characterized in that the formation of the source and drain regions comprises the deposition of a thick polycrystalline silicon encapsulating layer (27), the formation of a resin mask (28) on the thick polycrystalline silicon layer (27), the etching of the thick polycrystalline silicon layer

(27) by means of the mask to the desired shape and dimensions, the removal of the resin mask (28), the chemical-mechanical polishing of the thick silicon layer (23) down to level with the gate (15) in order to produce parts (23, 24) in the thick polycrystalline silicon layer (23) which are intended to form future source and drain regions co-planar with the gate and the implantation of a dopant in said parts (23, 24) in order to form the source and drain regions.

ABSTRACT

The invention concerns a semiconductor device comprises a silicon body (10) wherein are formed source and drain regions (23, 24) defining between them a channel region, a thin gate dielectric layer, a buried layer of dielectric material (22) extending between the source and drain regions (23, 24) and a thin silicon layer (13) extending between the source and drain regions and included between the buried dielectric material layer (22) and the gate dielectric layer (14). The invention is characterised in that said thin silicon layer (13) has an area greater than that of the gate dielectric layer (4) such that its upper surface comprises two opposite zones (13) extending beyond the gate dielectric layer (4) and the source and drain regions (8, 9) each respectively overlapping, at least partly, one of said opposite zones (13a). The invention is appicable to transistors.

FIG.1

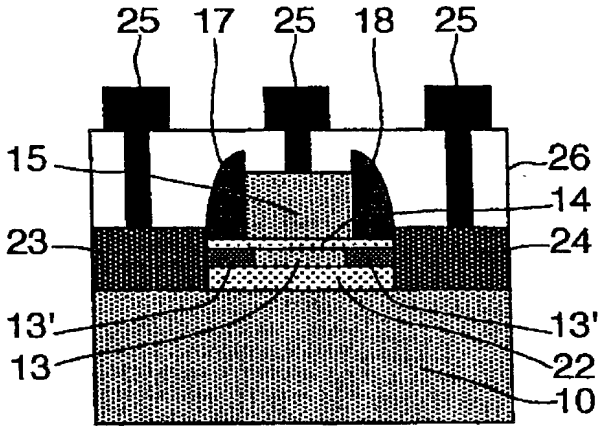


FIG.2

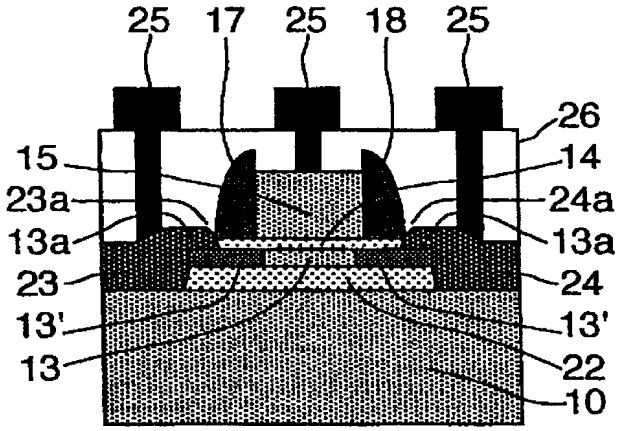


FIG.3

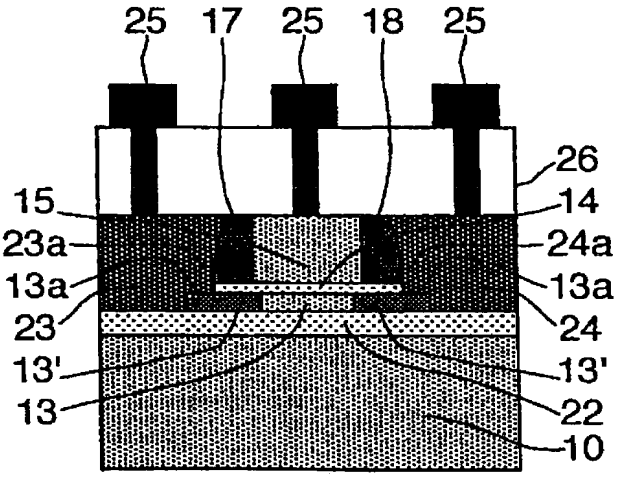


FIG.4a

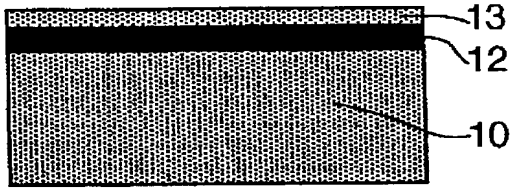


FIG.5a

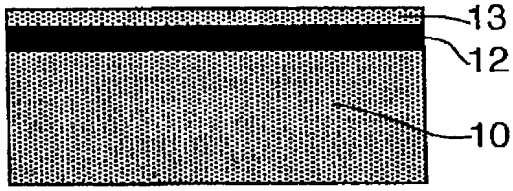


FIG.4b

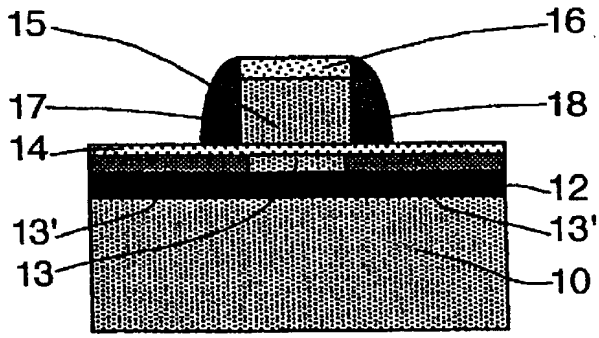


FIG.5b

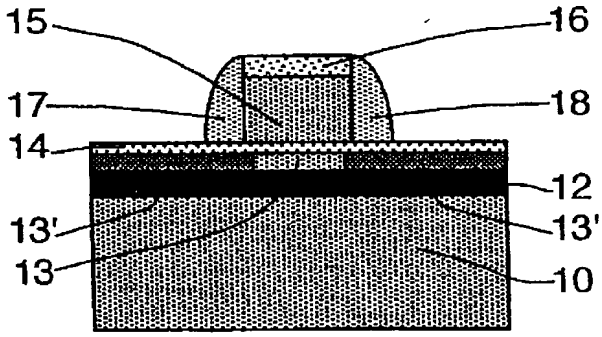


FIG.4c

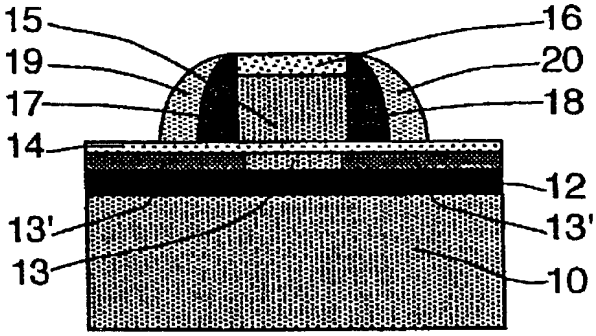


FIG.5c

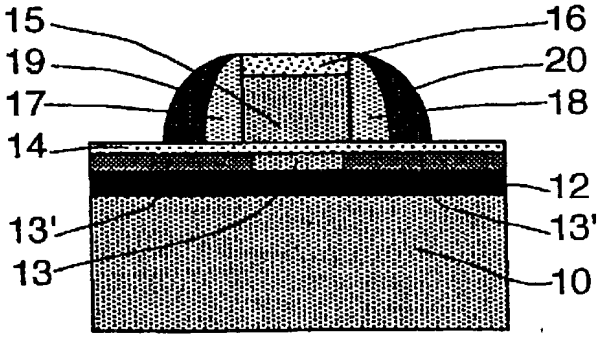


FIG.4d

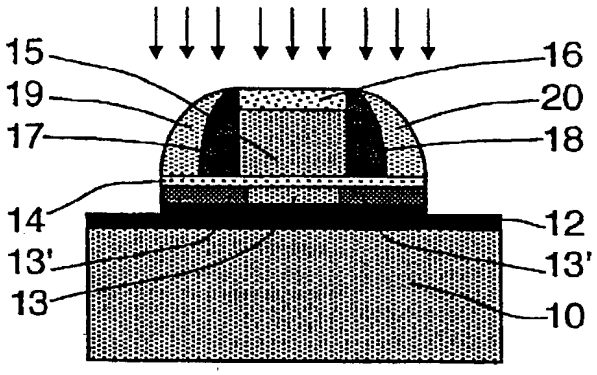


FIG.5d

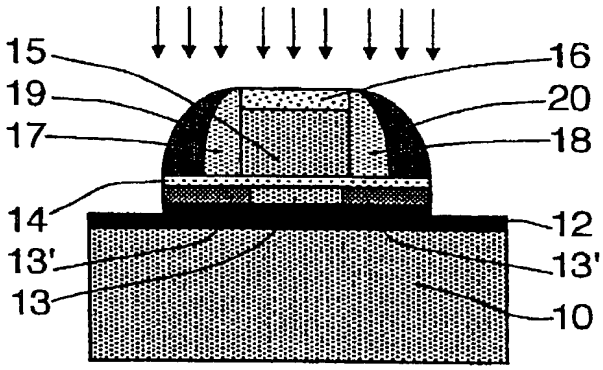


FIG.4e

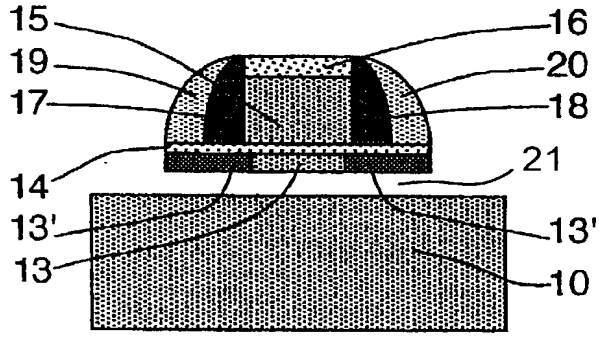


FIG.5e

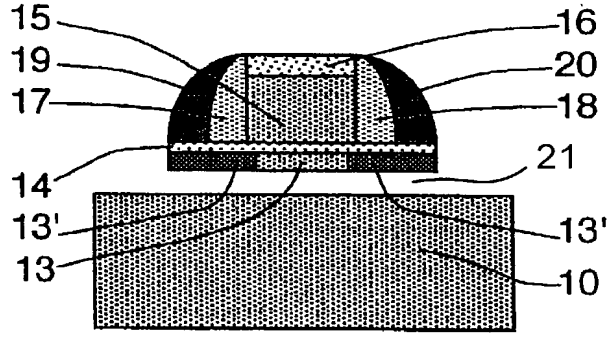


FIG.4f

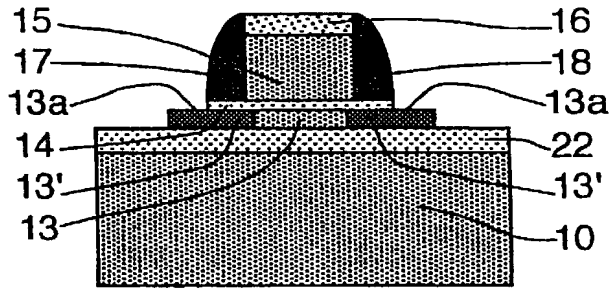


FIG.5f

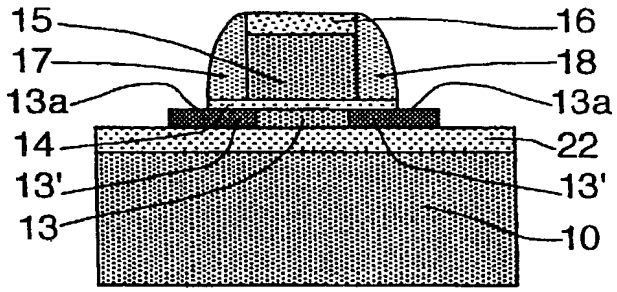


FIG.4f'

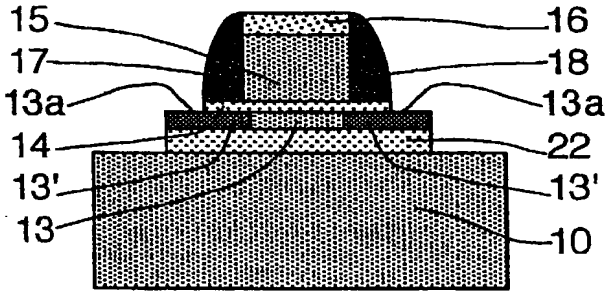


FIG.4g

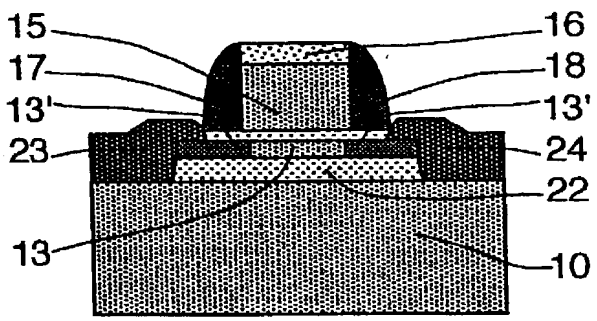


FIG.5g

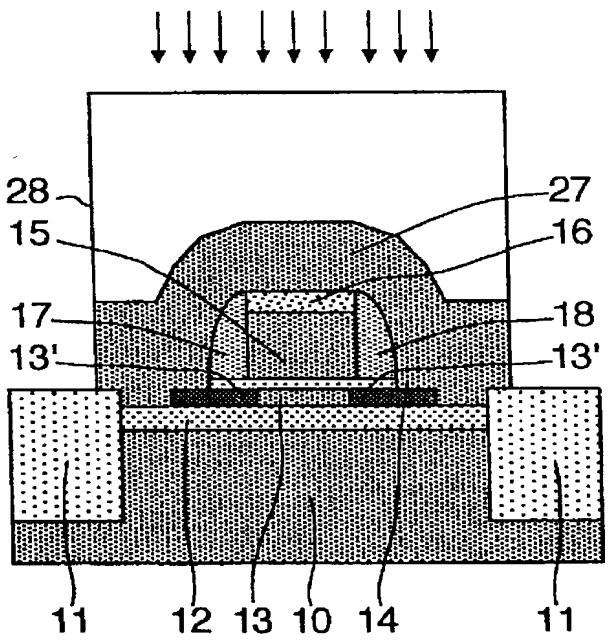


FIG.4h

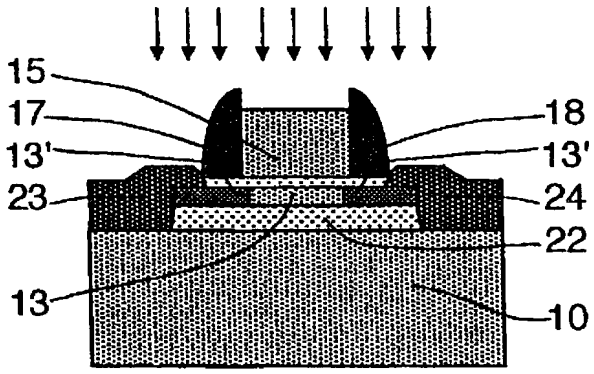


FIG.5h

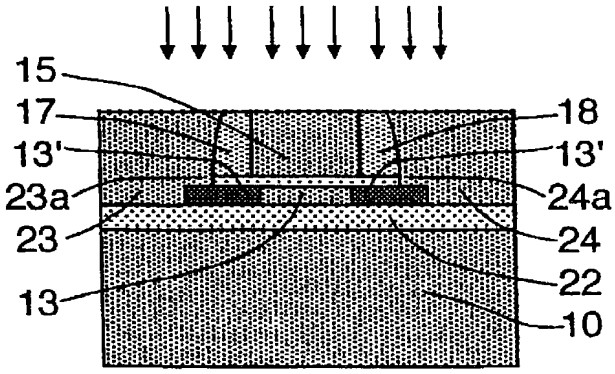
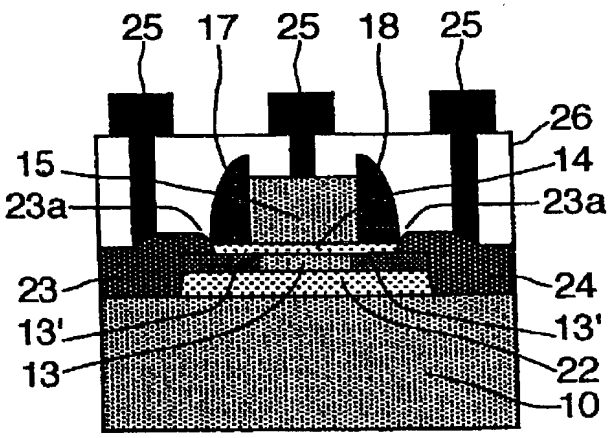


FIG.4i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17
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26
15
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23a
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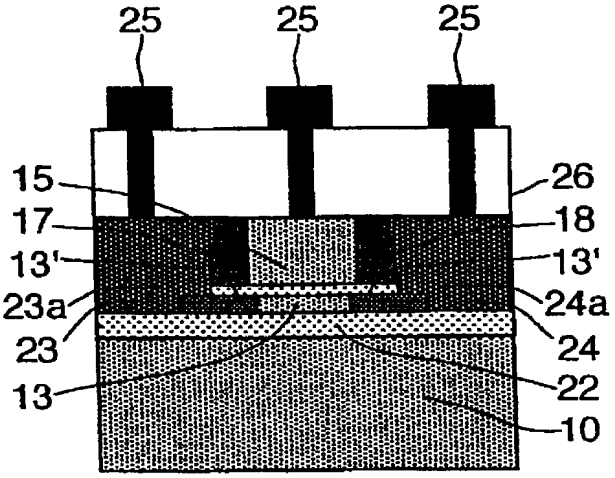
23
24
13'
13'
13
22
10

FIG.5i


25
25
25
15
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17
18
13'
13'
23a
24a
23
24
13
22
10

#4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/089,588
Filed: March 29, 2002
Inventor(s):
Bois et al.

Title: SEMICONDUCTOR DEVICE COMBINING THE ADVANTAGES OF MASSIVE AND SOI ARCHITECTURE, AND METHOD FOR MAKING SAME

Examiner: Unknown
Group/Art Unit: Unknown
Atty. Dkt. No: 5310-04500

CERTIFICATE OF EXPRESS MAIL
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Washington, D C. 20231

Derrick Brown

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned, being Assignee of record of the entire interest in the above-identified application by virtue of an assignment recorded in the United States Patent and Trademark Office as set forth below, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventors.

The Assignee hereby revokes any previous Powers of Attorney and appoints:

Mark K. Brightwell	Reg. No. 47,446
Brenna A. Brock	Reg. No. 48,509
Jason L. Burgess	Reg. No. 50,380
Gentry Crook	Reg. No. 44,633
Steve J. Curran	Reg. No. 50,664
Kevin L. Daffer	Reg. No. 34,146
Mark R. DeLuca	Reg. No. 44,649
Mollie E. Hamel	Reg. No. 48,405
Erik A. Heter	Reg. No. 50,652
Jeffrey C. Hood	Reg. No. 35,198
Robert C. Jahnke	Reg. No. 44,800
B. Noël Kivlin	Reg. No. 33,929
Robert C. Kowert	Reg. No. 39,255
Mark Lupkowski	Reg. No. 49,010
Lawrence J. Merkel	Reg. No. 41,191

(23)

Anne Marie Mewherter	Reg. No. 50,484
Eric B. Meyertons	Reg. No. 34,876
Louise K. Miller	Reg. No. 36,609
David W. Quimby	Reg. No. 39,338
Rory D. Rankin	Reg. No. 47,884
David A. Rose	Reg. No. 26,223
Doug M. Shamah	Reg. No. 45,093
Mark S. Williams	Reg. No. 50,658

each an attorney or agent of the firm of CONLEY, ROSE & TAYON, P.C., as its attorney or agent for so long as they remain with such firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned has reviewed the evidentiary documents, specifically the Assignment to France Telecom, referenced below, and certify that to the best of my knowledge and belief, title remains in the name of the Assignee.

Please direct all communications as follows:

Eric B. Meyertons, Esq.
CONLEY, ROSE & TAYON, P.C.
P.O. BOX 398
AUSTIN, TEXAS 78767-0398
(512) 476-1400 (voice)
(512) 703-1250 (facsimile)

ASSIGNEE:

FRANCE TELECOM

FRANCE TELECOM 6, place d'Alleray 75015 PARIS

By: Didier LEMOYNE

Corporate Patents Manager

Title:

Date: June 18, 2002

ASSIGNMENT: x Enclosed for recording

#4

DECLARATION AND POWER OF ATTORNEY
U.S.A.

Attorneys' Docket n°

As a below named inventor, I hereby declare that :

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original , first and sole inventor (if only one name is listed below), or the below named inventors believe they are the original, first and joint inventors (if plural names are listed below) , of the subject matter which is claimed and for which patent is sought on the invention entitled : **SEMICONDUCTOR DEVICE COMBINING THE ADVANTAGES OF MASSIVE AND SOI ARCHITECTURE, AND METHOD FOR MAKING SAME.**

which is described and claimed in

(X) PCT International Application N° **PCT/FR00/02710** filed **29 September 2000**
( ) the attached specification
(X) the specification in application Serial No. 10/089,588 of March 29, 2002
and was amended on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims , as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent Office all information known to me to be material to patentability of the subject matter claimed in this application , as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code , § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having filing date before that of the application on which priority is claimed :

Foreign/PCT Appln. N°	Country	Filing Date	Priority Claimed (Yes / No)
99/12308	France	1st October 1999	Yes

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) or any PCT international application(s) designating the United States listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information known to me to be material to the patentability of the subject matter claimed in this application , as "materiality" is defined in Title 37, Code of Federal Regulations, §1.56 which become available between the filing date of the prior application and the national or PCT International filing date of this application :

U.S.Application N°	Filing Date	Status (patented/pending/abandoned)

Please direct all communications as follows :

Eric B.Meyertons
Conley, Rose & Tayon, P.C.
P.O. Box 398
Austin , Texas 78767-0398
Ph. (512) 476-1400

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true ; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code; and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

==========

1-00

Full name of sole or first inventor : Daniel BOIS

Citizenship : French

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Signature : _____ **Date :** June 18, 2002

Daniel BOIS

2-00

Full name of second joint inventor : Thomas SKOTNICKI

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Signature : T. Skotnicki **Date :** June 18,, 2002

Thomas SKOTNICKI

3-00

Full name of third joint inventor : Malgorzata JURCZAK

Citizenship : Polish

Residence (City,State,Country) :Grenoble, France FRX

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Signature : M. Jurczak **Date :** June 18, 2002

Malgorzata JURCZAK